

E-FILED on 10/22/07

IN THE UNITED STATES DISTRICT COURT  
FOR THE NORTHERN DISTRICT OF CALIFORNIA  
SAN JOSE DIVISION

COMPUTER CACHE COHERENCY  
CORPORATION,

Plaintiff,

v.

VIA TECHNOLOGIES, INC. and VIA  
TECHNOLOGIES, INC. (USA),

Defendants.

No. C-05-01668 RMW

ORDER ON CLAIM CONSTRUCTION AND  
ASSOCIATED MOTION FOR SUMMARY  
JUDGMENT OF INVALIDITY BASED ON  
INDEFINITENESS

**[Re Docket Nos. 45, 52, 63, 94]**

COMPUTER CACHE COHERENCY  
CORPORATION,

Plaintiff,

v.

INTEL CORPORATION,

Defendant.

No. C-05-01766 RMW

ORDER ON CLAIM CONSTRUCTION

**[Re Docket Nos. 66, 71, 74]**

(Cases consolidated for claim construction)

The parties briefed the issue of construction of U.S. Patent No. 5,072,369 ("the '369 patent") and filed several motions for summary judgment. The court held a claim construction hearing which included a tutorial and heard argument on claim construction and the summary judgment motions.

ORDER ON CLAIM CONSTRUCTION AND ASSOCIATED MOTION FOR SUMMARY JUDGMENT OF INVALIDITY BASED ON INDEFINITENESS—No. C-05-01668 RMW; No. C-05-01766 RMW  
JAH/MAG

1 After considering the positions of all parties, the court construes the terms at issue and rules on the  
2 Via's motion for summary judgment of invalidity of the '369 patent for indefiniteness (docket no.  
3 94), which presents an issue that is intertwined with claim construction. A separate order will be  
4 issued on the remainder of the summary judgment motions.

### 5 I. BACKGROUND

6 The '369 patent discloses an interface circuit that permits devices connected to two different  
7 buses to utilize a main memory on one of the two buses, where the main memory on that bus has a  
8 cache memory. The invention purports to solve, in the context of two buses, a "cache coherency"  
9 problem wherein a device requesting data from memory that has been cached is able to access the  
10 most current data in memory, whether that data is stored in main memory or in cache memory.  
11 Specifically, the patent describes the cache coherency problem in the context of a single bus as  
12 follows:

13 To provide faster memory access, a computer processor on the bus may copy a block  
14 of data from an area of the low speed main memory into a higher speed cache  
15 memory and thereafter read and write access the data in the cache memory rather than  
16 in main memory. However, if another computer processor on the bus subsequently  
17 read accesses the same area of main memory, data read may be "obsolete" because it  
18 was not updated when corresponding data stored in cache memory was updated.  
19 Also, if another computer processor on the bus writes data to the area of main  
20 memory, corresponding data in cache memory becomes obsolete.

21 '369 patent at 1:25-35.

22 Plaintiff Computer Cache Coherency Corporation ("CCCC") owns by assignment the '369  
23 patent and has sued defendants Via Technologies, Inc. and Via Technologies, Inc. (USA)  
24 (collectively, "Via") in one action for infringing the '369 patent, and similarly has sued defendant  
25 Intel Corporation ("Intel") in another action. The defendants filed counterclaims seeking a  
26 declaratory judgment that the '369 patent is invalid, unenforceable, and not infringed. These two  
27 actions have been consolidated for claim construction.

28 CCCC asserts only the rather lengthy first claim of the '369 patent in this action. Claim 1  
reads:

An apparatus for providing data communication between first and second buses,  
the first bus providing a first plurality of bus masters connected thereto with data  
read and write access to first data storage locations mapped to separate addresses

within a first address space, wherein one of said first plurality of bus masters writes data to a first particular one of said first data storage locations by placing on the first bus an address to which the first particular one of said first data storage locations is mapped and transmitting the data via said first bus, and wherein one of said first plurality of bus masters reads data from a second particular one of said first data storage locations by placing on the first bus an address to which the second particular one of said first storage locations is mapped and receiving data via said first bus,

the second bus providing a second plurality of bus masters connected thereto with data read and write access to second data storage locations mapped to separate addresses within a second address space, wherein one of said second plurality of bus masters writes data to a first particular one of said second data storage locations by placing on the second bus an address to which the first particular one of said second data storage locations is mapped and transmitting the data via said second bus, and wherein one of said second plurality of bus masters reads data from a second particular one of said second data storage locations by placing on the second bus an address to which the second particular one of said second storage locations is mapped and receiving data via said second bus,

wherein one of said second plurality of bus masters connected to said second bus caches data read out of a subset of said second data storage locations, said second bus including means for conveying a SNOOP signal with an address appearing on the bus, the SNOOP signal telling said one of said second plurality of bus masters when to write cached data to the address appearing on the bus,

the apparatus comprising:

first mapping means coupled to said first bus for mapping first addresses within the first address space to second addresses within the second address space, for asserting an indicating signal and for generating one of said second addresses in response to one of said first addresses transmitted on said first bus from one of said first plurality of bus masters, said first mapping means also generating a SNOOP signal of a state indicating when a generated second address is mapped to one of said particular subset of the second data storage locations, and

bus interface means connected to said first and second buses for responding to the first indicating signal when said one of said first plurality of bus masters is reading data by placing the generated second address and SNOOP signal on the second bus, receiving data from a second data storage location mapped to said second address, and transmitting the received data to said one of said first plurality of bus masters via said first bus when the said one of said first plurality of bus masters is reading data.

## II. ANALYSIS

### A. Preamble

As a preliminary matter, the parties dispute whether the preamble to the claim is limiting. CCCC contends that the court need not decide whether the preamble of claim 1 is limiting because the two terms from the preamble that the defendants seek to have construed need no construction; this assertion is CCCC's entire opposition to whether the preamble of claim 1 is limiting. However,

whether terms of the preamble need to be construed is a separate issue from whether the preamble is limiting; plain language that needs no construction is still capable of being a claim limitation.

"Whether to treat a preamble as a claim limitation is determined on the facts of each case in light of the claim as a whole and the invention described in the patent." *Storage Technology Corp. v. Cisco Systems, Inc.*, 329 F.3d 823, 831 (Fed. Cir. 2003). A preamble may limit the invention if it "recites essential structure or steps, or if it is necessary to give life, meaning, and vitality to the claim." *Catalina Mktg. Int'l v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002). Further, "dependence on a particular disputed preamble phrase for antecedent basis may limit claim scope because it indicates a reliance on both the preamble and claim body to define the claimed invention." The preamble also limits claim scope "when the preamble is essential to understand limitations or terms in the claim body" or "when reciting additional structure or steps underscored as important by the specification." *Id.*

A preamble is not limiting, however, "where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention." *Id.* Thus, "a preamble generally is not limiting when the claim body describes a structurally complete invention such that deletion of the preamble phrase does not affect the structure or steps of the claimed invention" or where the preamble "extoll[s] benefits or features of the claimed invention." *Id.* at 809 Further, "preambles describing the use of an invention generally do not limit the claims because the patentability of apparatus or composition claims depends on the claimed structure, not on the use or purpose of that structure." *Id.*

The preamble of claim 1 of the '369 patent describes the two buses and attached devices that are the setting in which the "interface circuit," the apparatus explicitly claimed, functions. The preamble could thus be seen as merely explaining the use of the claimed apparatus, favoring a finding that the preamble is not limiting. However, the preamble is longer than the claim body. Compare '369 patent at 12:41-13:14 with *id.* at 13:15-14:12. Several terms in the claim body—such as "said first bus," "the first address space," "the second address space," "said first plurality of bus masters," "SNOOP signal," and "said particular subset of the second data storage locations"—have their antecedents in the preamble. For example, to literally infringe, a "first mapping means" must

be "coupled to said first bus" in an accused device. *See* '369 patent at 13:16. Likewise, the "bus interface means" has to be "connected to said first and second buses." *Id.* at 14:3-4. Any accused device must be so "coupled" and "connected" but cannot be without the first and second buses described in the preamble. The claim body is not structurally complete without reference to the preamble. Thus, the preamble is necessary to give meaning to claim 1 and is therefore limiting.

## **B. Construction of Specific Terms and Phrases**

A court's claim construction analysis begins with the words of the claim. *Nystrom v. Trex Co., Inc.*, 424 F.3d 1136, 1142 (Fed. Cir. 2005). For each term to be construed, the court must determine "the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (*en banc*).

### **1. "Bus"**

<i>Term</i>	<i>VIA &amp; Intel's Proposal</i>	<i>CCCC's Proposal</i>
"bus"	"A set of parallel conductors that is capable of transmitting signals between two or more modules (such as computer processors and local memories) connected to these conductors."	"One or more conductors used for transmitting signals or power from one or more sources to one or more destinations."

#### **i. Serial or Parallel**

The parties' primary disagreement about the term "bus" is whether, as used in the patent, "bus" refers to any sort of bus, or only a parallel bus.<sup>1</sup> One definition of bus circa 1998, as provided by IEEE, is as CCCC proposes: "one or more conductors used for transmitting signals or power from one or more sources to one or more destinations." Buses may be classified as either

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<sup>1</sup> Because from the parties' original filings and arguments it was unclear the precise definition of "parallel bus" that one skilled in the art would have used in the context of the '369 patent at the time its application was filed, the court ordered the parties to file supplemental declarations on the definitions of "parallel bus" and the related term "serial bus," as well as certain other bus-related terms the parties believed would be helpful to the court to understand. From the supplemental declarations the parties filed, it appears that they generally agree on the applicable definitions of "parallel bus" and "serial bus." In its filing in response to the court's order, Salik Decl. (dkt. # 198), CCCC included in its declaration information beyond that requested by the court. Defendants also object on several grounds—such as relevance, and lack of factual support—to CCCC's supplemental declaration. Defendants' objections are all well-taken and sustained.

"serial" or "parallel." Levy Decl. (dkt. # 130<sup>2</sup>) ¶¶ 3-4. A parallel bus is one containing more than one conductor used simultaneously to transmit data, while a serial bus has only one conductor for data. *Id.* ¶¶ 5-6.

The dispute over whether the construction of bus is limited to parallel buses is informed by reviewing the use of "bus" and "parallel bus" in the specification. CCCC argues that since the term "parallel bus" appears in certain places in the patent, the drafter clearly intended "bus" alone to not be limited to a parallel bus. Defendants, on the other hand, contend that all uses of "bus" refer to "parallel buses."

The defendants are correct that at least some uses of "bus" necessarily refer to a parallel bus. For example, the background section of the patent states:

When various computer processors employ differing parallel buses, it is not possible to directly connect the computer processors to the same bus. In such case, the processors must operate within separate computer systems utilizing separate buses and accessing separate local memories.

'369 patent at 1:53-58. The first sentence contemplates a situation involving "differing parallel buses," and the second sentence, in explaining the limitations of such a situation, refers merely to "buses," even though these "buses" are those discussed in the first sentence and as a result, necessarily parallel. However, the background section specifies parallel buses twice, but mentions buses without further specification eleven other times.

It is not clear that each mention of "bus" should be taken to be a reference to a parallel bus. For example, the background section begins with the sentence: "[t]he present invention relates in general to interface circuits providing communication between computer systems and in particular to an interface circuit permitting a bus master connected to one computer bus to directly access data stored in a memory connected to another bus." '369 patent at 1:10-15. This sentence does not clearly refer only to parallel buses.

Defendants nevertheless argue that the patent's references to "bus" refers to parallel buses. First, they argue that the specification sets forth the problem to be solved in the prior art only in

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<sup>2</sup> This declaration was docketed only in case C-05-01766. All other references to docket numbers in this order are those used for case C-05-01668

terms of parallel buses. However, the problem to be solved need not necessarily limit the patent claims. *See, e.g., Brookhill-Wilk I, LLC v. Intuitive Surgical, Inc.*, 334 F.3d 1294, 1301 (Fed. Cir. 2003). Further, it does not appear that the patentee has acted as his own lexicographer, providing a clear definition of "bus" as a parallel bus. *See Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1094-95 (Fed. Cir. 2003) (references to "multiplexed bus" in specification does not limit "bus" as used in claims to a "multiplexed bus"); *Multiform Desiccants Inc. v. Medzam Ltd.*, 133 F.3d 1473, 1477 (Fed. Cir. 1998) (any special meaning assigned to a term "must be sufficiently clear in the specification that any departure from common usage would be so understood by a person of experience in the field of the invention."). Nor does it appear that the defendants' narrower construction of "bus" is necessary to preserve the validity of the claim. As CCCC points out, the problem of cache coherency is not necessarily limited to the parallel buses, even if the problem to be solved and preferred embodiment are stated in the context of parallel buses. Thus, because the patent specification refers to both "buses" and "parallel buses" and because there is no special definition of "bus" clearly defined in the specification, the court concludes that "bus" is not limited solely to a parallel bus.

## ii. Signal or Power

The parties also disagree as to whether "bus" should be defined as transmitting signals only or "signals or power." The patent clearly contemplates information passing through the bus, so it is undisputed that a bus transmits signal. The patent does not disclose power passing through the bus.

CCCC's proposed construction, using "signals or power," is too broad because it would allow a bus that is only used for transmitting power and not signal. While it is true that a signal, which is an electrical current, carries power, albeit a very small amount ( $P = I^2R$  or power = current squared multiplied by resistance), defining the term as transmitting either "signal or power" implies that the bus can solely transmit power, which is not disclosed. Therefore, although it is implicitly understood that a signal carries power, it should not be defined to be "signal or power."

## iii. Transmission

CCCC proposes the use of one of many available IEEE dictionary definitions to construe "bus." Defendants argue that in light of the Federal Circuit in *Phillips*, it is inappropriate to just

select the broadest possible dictionary definition. The focus is on how the particular claim term is used in the patent claims and specification. Upon review of the available IEEE definitions circa 1998, IEEE definition number 2, which relates to a "microcomputer system bus," defines "bus" to be "a signal line or set of lines used by an interface system to connect a number of devices and to transfer information." *See* Salik Decl. (dkt. # 46), Ex. 10. This definition of bus, which describes a shared bus, is more appropriate in light of the claim language. The preamble specifies "the first bus providing a first plurality of bus masters connected thereto", '369 patent at 12:43-4, and "the second bus providing a second plurality of bus masters connected thereto", '369 patent at 12:58-9. It is thus clear from the claim language that the patent contemplates shared buses—buses that are connected to a plurality of bus masters such that the buses connect multiple devices—and not buses that connect a single source to a single destination. Indeed, all uses of "bus" in the claims and the specification of the '369 patent describe a shared structure to which multiple bus masters are connected.

#### iv. Construction

Based on the foregoing, the court construes "bus" as "a signal line or set of signal lines used by an interface system to connect a number of devices and to transfer information between the devices." The parties have agreed that the construction of "first bus" and "second bus" follows the construction of "bus."

#### 2. "Address Space"

<i>Term</i>	<i>VIA &amp; Intel's Proposal</i>	<i>CCCC's Proposal</i>
"address space"	"A set of addresses that may be represented on a particular bus."	"A set of addresses that may be associated with one or more buses."

According to Claim 1, each "bus" provides "bus masters connected" to it with access to "data storage locations mapped to separate addresses within" an "address space." '369 patent at 12:43-46, 58-61. The parties agree that "address" means "an identification, such as a label, number, or name that designates a particular location in storage or any other data destination or source." Accordingly, the court will construe "address space" as "a set of addresses."

But as demonstrated by the parties' differing proposed constructions, the real dispute is over whether the first address space must be associated with the first bus and the second address space must be associated with the second bus. Basically, the parties disagree whether an address space is necessarily associated with only one bus or may be associated with multiple buses. The language of the patent resolves this disagreement. The description of the preferred embodiment makes clear that, at least for the preferred embodiment, each address space is associated with only one bus:

The interface circuit **8** maps a portion of VMEbus address space onto a portion of Futurebus address space so that when computer **2** read or write accesses selected addresses on the VMEbus, the interface circuit **8** implements the read or write access on corresponding addresses in a device on Futurebus **12** such as main memory **3**.

'369 patent at 3:35-41. However, limitations from the preferred embodiment may not be read into the claims. *Primos, Inc. v. Hunter's Specialties, Inc.*, 451 F.3d 841, 848 (Fed. Cir. 2006).

Nevertheless, the claims discuss the first address space along with the first bus and components connected to the first bus. The preamble to claim 1 sets forth a *first* bus providing a *first* plurality of bus masters to *first* data storage locations mapped to separate addresses within a *first* address space. In identical fashion, the second address space is discussed along with the second bus and components attached to the second bus; the preamble sets forth a *second* bus providing a *second* plurality of bus masters to *second* data storage locations mapped to separate addresses within a *second* address space. This discussion clearly demonstrates that an "address space" when modified by either "first" or "second" is associated with the corresponding bus.<sup>3</sup>

Based on the foregoing, the court construes "address space" as "a set of addresses." Further, the court construes "first address space" as an address space that necessarily refers to addresses represented on the first bus and "second address space" as an address space that necessarily refers to addresses represented on the second bus.

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<sup>3</sup> There is a portion of the claims from which it might appear that a "first" reference is used inconsistently with the association set forth above. At column 12 lines 58-67, the patent reads, "the second bus providing a second plurality of bus masters connected thereto with data read and write access to second data storage locations mapped to separate addresses within a second address space, wherein one of said second plurality of bus masters writes data to a *first* particular one of said second data storage locations by placing on the second bus an address to which the first particular one of said second data storage locations is mapped and transmitting the data via said second bus." The "first particular one" is not inconsistent because it refers to the first of a number of second data storage locations that are mapped on the second address space.

### 3. "SNOOP Signal"

<i>Term</i>	<i>VIA &amp; Intel's Proposal</i>	<i>CCCC's Proposal</i>
"SNOOP signal"	"A signal indicating whether a generated second address references a cached data storage location."	"A signal that triggers a determination of whether the data corresponding to an address in cacheable memory is cached."

The main dispute between the parties appears to be whether a "SNOOP signal" indicates whether an address refers to a cached memory or whether it merely triggers that determination. The proper construction of SNOOP signal can be ascertained by reviewing the specification and asserted claim of the patent. First, in the Background section of the patent, the term SNOOP signal is introduced in the context of prior art where a bus master asserts a SNOOP signal on a single bus to check whether "a second bus master [. . .] is using a cache memory for data stored at that memory address." '369 patent at 1:36-45. Next, the Summary section explains in the context of a two-bus system that the SNOOP signal is a signal "indicating whether the Futurebus address references a cached data storage location on the Futurebus." '369 patent at 2:19-30. This portion of the Summary makes it clear that two buses are involved: the first address originates from the VMEbus and the Futurebus address corresponds to a second address. Finally, in the claims, SNOOP is again defined as a signal "indicating when a generated second address is mapped to one of said particular subset of the second data storage locations." '369 patent at 13:23-14:2. This language is consistent with that set forth in the Summary section. In either the context of single bus (prior art) or two buses (the invention), the SNOOP signal indicates whether an address references a cached storage location, it does not merely trigger a determination whether data is cached.

Defendants' proposed claim construction seeks to limit a SNOOP signal to determining whether a "second generated address" references a cached location. However, as plaintiff points out, part of the claim specifies that the first mapping means generates "a SNOOP signal of a state indicating when a generated second address is mapped to one of said particular subset of the second data storage locations." '369 patent at 13:24-14:12. Because this portion of the claim specifies that a SNOOP signal must be in a particular state "indicating when a generated second address is mapped" to a cached location, it cannot be that the general definition of SNOOP signal must always include determining whether a "second generated address" references a cached location. However, although

the construction of term "SNOOP signal" is not limited to indicating whether a second generated address references a cached data storage location, the language of the claim itself requires the first mapping means to generate a SNOOP signal with the particular "state indicating when a generated second address is mapped to one of said particular subset of second data storage locations." '369 patent at 13:23-14:2.

Based on the foregoing, the court construes "SNOOP signal" as "a signal indicating whether an address references a cached data storage location."

<i>Term</i>	<i>VIA &amp; Intel's Proposal</i>	<i>CCCC's Proposal</i>
"the SNOOP signal telling said one of said second plurality of bus masters when to write cached data to the address appearing on the bus"	"The SNOOP signal indicating to one of the bus masters on the second bus when to write cached data to one of the second data storage locations at the address appearing on the bus."	"The SNOOP signal indicating to a bus master when it may be required to write cached data to the address appearing on the second bus."

The language here, "the SNOOP signal telling said one of said second plurality of bus masters when to write cached data to the address appearing on the bus," is describing actions taking place on the second bus, as illustrated in the bottom portion of Fig. 1. To properly construe this language, however, it is necessary to look at the context in which the disputed language arises.

This disputed language (underlined below) appears as part of a wherein clause in the preamble. The antecedent basis for this wherein clause is found in the prior paragraph of the claim preamble. Together these paragraphs read:

the second bus providing a second plurality of bus masters connected thereto with data read and write access to second data storage locations mapped to separate addresses within a second address space, wherein one of said second plurality of bus masters writes data to a first particular one of said second data storage locations by placing on the second bus an address to which the first particular one of said second data storage locations is mapped and transmitting the data via said second bus, and wherein one of said second plurality of bus masters reads data from a second particular one of said second data storage locations by placing on the second bus an address to which the second particular one of said second storage locations is mapped and receiving data via said second bus,

wherein one of said second plurality of bus masters connected to said second bus caches data read out of a subset of said second data storage locations, said second bus including means for conveying a SNOOP signal with an address appearing on the bus, the SNOOP signal telling said one of said second plurality of bus masters when to write cached data to the address appearing on the bus

'369 patent at 12:58-13:13 (emphasis added).

It is clear from the claim language that the SNOOP signal indicates to one of the bus masters on the *second bus* when to write cached data to an address appearing on the second bus. This is nearly a direct transcription of the claim language "wherein one of said second plurality of bus masters connected to said second bus." '369 patent at 13:6-7. But there appears to an issue regarding whether the cached data writing is limited to the *second data storage locations* on the second bus. Defendants correctly argue that because the "wherein" clause describes the SNOOP signal on the "second bus" to which the "second plurality of bus masters" that cache data read out of "second data storage locations" is connected, it must follow that "the address appearing on the bus" immediately preceding the disputed claim term should also be construed to originate from a device on the second bus. Thus, in light of the preceding paragraph of the preamble, the court concludes that the claim requires that a SNOOP signal indicate to the bus master on the second bus when to write cached data to the corresponding second storage location at the address on the second bus.

Accordingly, the court construes the language "the SNOOP signal telling said one of said second plurality of bus masters when to write cached data to the address appearing on the bus" as saying "the SNOOP signal indicating to one of the bus masters on the second bus when to write cached data to the one of the second data storage locations at the address appearing on the second bus."

<i>Term</i>	<i>VIA &amp; Intel's Proposal</i>	<i>CCCC's Proposal</i>
"a SNOOP signal of a state indicating when a generated second address is mapped to one of said particular subset of the second data storage locations"	"a SNOOP signal of a state indicating when the generated second address belongs to the particular subset of the second data storage locations."	"A SNOOP signal of a state indicating that a bus master has accessed an address that maps to a particular subset of the second data storage locations."

Based upon the foregoing constructions of "SNOOP signal," "second," and "mapped," no further construction of this language is necessary.

<i>Term</i>	<i>VIA &amp; Intel's Proposal</i>	<i>CCCC's Proposal</i>
"said second bus including means for conveying a SNOOP signal with an address appearing on the bus"	This phrase should be construed in accordance with 35 U.S.C. § 112 6. The function is "conveying a SNOOP signal with an address appearing on the bus." The corresponding structure is the Futurebus as illustrated in Figures 1 and 2, reference numeral 12. The claim limitation covers this corresponding structure and its equivalents.	Plaintiff does not believe that this phrase should be read as a "means-plus-function" clause in accordance with 35 U.S.C. § 112(6), because the claim identifies sufficient structure for performing the recited function, namely, the "second bus." If construed as a "means-plus-function" clause in accordance with 35 U.S.C. § 112(6), plaintiff proposes the corresponding structure consists of a conductor or conductors within the second bus.

To begin with, the parties dispute whether "means for conveying" should be construed as a means-plus-function limitation. A claim limitation containing the word "means" is presumptively a means-plus-function limitation. *Sage Prods. v. Devon Indus.*, 126 F.3d 1420, 1427 (Fed. Cir. 1997). Nevertheless, CCCC contends that "means for conveying" need not be construed as a means-plus-function term because a bus inherently includes the structure for conveying a signal. Specifically, CCCC argues:

[b]y definition, a bus includes one or more conductors for transmitting signals. Because a bus inherently has structure sufficient for conveying a signal (namely, a conductor), the recited second bus inherently has the structure sufficient for performing the identified function. No need exists to look to the specifications for additional structure.

CCCC Claim Constr. Br. (dkt. # 45) at 19. The court agrees that a bus has a means for conveying signal, but that is not all that the disputed term requires; it also requires a means for conveying a *SNOOP signal*, or a particular type of signal. As a means for conveying a SNOOP signal is not inherent in a bus, the court proceeds to the required analysis for a means-plus-function limitation.

The parties dispute exactly what the "means for conveying" is. As the Federal Circuit has explained, "Claim construction of a means-plus-function limitation includes two steps. First, the court must determine the claimed function. Second, the court must identify the corresponding structure in the written description of the patent that performs that function." *Applied Med. Res. Corp. v. U.S. Surgical Corp.*, 448 F.3d 1324, 1332 (Fed. Cir. 2006) (citations omitted).

The first step, identifying the function, is simple. The parties do not dispute that the function of the "means" is precisely what claim 1 recites: "conveying a SNOOP signal with an address appearing on the bus." The second step, identifying the corresponding structure, is the subject of the parties' disagreement. Defendants argue that because the only embodiment of the "second bus" disclosed in the specification is the "Futurebus," the structure associated with "means for conveying" must be taken to be the Futurebus.

The resolution to the disputed construction appears in the preamble, which describes that requirement of having a first and second bus. The disputed language of the claim limits the second bus to one that includes means for conveying a SNOOP signal. In the preferred embodiment, this means for conveying a SNOOP signal is the Futurebus. The Futurebus was known in the art as a bus capable of conveying a SNOOP signal. Therefore court identifies the structure of the "means for conveying a SNOOP signal with an address appearing on the bus" the Futurebus and its equivalents."

#### 4. "Mapping"

<i>Term</i>	<i>VIA &amp; Intel's Proposal</i>	<i>CCCC's Proposal</i>
"mapping"	"Translating"	"Establishing a correspondence between the elements of one set and elements of another set."

The parties agree that "mapped" means "established correspondence between the elements of one set and the elements of another set." Nevertheless, defendants propose construing "mapping" as "translating."

Defendants face an uphill battle to show that "mapping" should not be construed in an analogous fashion to "mapped" because "claim terms are normally used consistently throughout the patent."<sup>4</sup> *Phillips*, 415 F.3d at 1314. The prosecution history of U.S. Patent No. 5,088,028, to which defendants cite, is of questionable relevance when construing the terms of the '369 patent because

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<sup>4</sup> Intel's citation to *Comark Communications v. Harris Corp.*, 156 F.3d 1182, 1187 (Fed. Cir. 1998) ("There is presumed to be a difference in meaning and scope when different words or phrases are used in separate claims."), does not support Intel's argument that "the patent uses the terms 'mapping' and 'translating' synonymously." See Intel Opp'n (dkt. # 71) at 16. In *Comark*, the Federal Circuit held that a term in an independent claim should presumptively not be defined in such a way as to render a dependent claim "completely superfluous and redundant." *Id.*

the two patents, although having similar specifications, were not formally related.<sup>5</sup> See *Goldenberg v. Cytogen, Inc.*, 373 F.3d 1158, 1167-68 (Fed. Cir. 2004). While "mapping" and "translating" both appear in the patent, they are not, as defendants assert, used as synonyms. The description of the preferred embodiment contains the following language:

When a device on VMEbus **10** seeks to read or write access an address mapped to Futurebus address space, a VMEbus-to-Futurebus (V-F) translation circuit **18**, coupled to VMEbus **10** by a buffer **20**, translates the upper portion A(12:31) to a corresponding upper portion of the Futurebus bus address, and a buffer **22** selectively places this portion of the Futurebus address on local address bus **16**.

'369 patent at 4:11-18. In the context this passage, it appears that VMEbus addresses have already been mapped to Futurebus addresses ("When a device on VMEbus seeks to read or write access an address mapped to Futurebus address space"), but that the translating must be done each time a device on the VMEbus wishes to access a mapped address ("a [V-F] translation circuit . . . translates the upper portion . . . to a corresponding upper portion of the Future bus address"). The patent thus makes clear that mapping and translating in some instances take place at different times and therefore cannot be synonyms. The court adopts CCCC's proposed construction of "mapping" because it is consistent with both the parties' agreed-upon definition of "mapped" and the language of the patent. "Mapping" is "establishing a correspondence between the elements of one set and elements of another set."

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<sup>5</sup> The court understands defendants' argument that as a matter of policy, a patentee should not be able to benefit from improperly failing to alert the PTO to the fact that on the same day, the same inventors filed two separate patent applications containing substantially overlapping specifications and claim language. (The application for the '369 patent and the parent application of the '028 patent were both filed on April 7, 1989.) Even assuming the defendants are correct that the '369 and '028 patents should have been related during prosecution and that the prosecution history of the '028 could therefore in theory be used to narrow the scope of the '369 patent, the argument of the patentee they quote,

Applicants' claimed invention is an interface circuit 8 for communicating between two computer systems having respective bus masters (2;4) and system buses (10;12), the two systems having different protocols, such as VMEbus and Futurebus. An address on the first bus intended for a device on the second bus is detected and translated into an address on the second bus by V-F translator 18 and address generator 47 while a first local bus request signal V-LREQ is generated, Ochs Decl. (dkt. # 54), Ex. 4 at 5, is consistent with mapping taking place once initially and translating taking place each time cross-bus access is sought. The court therefore need not try to predict whether the Federal Circuit would, upon consideration of the facts of this case, expand the rule of *Goldenberg* to cover the instant situation.

<b>Term</b>	<b>VIA &amp; Intel's Proposal</b>	<b>CCCC's Proposal</b>
"mapping first addresses within the first address space to second addresses within the second address space"	"Translating first addresses within the first address space to second addresses within the second address space."	"establishing a correspondence between a first address within a first address space to a second address within a second address space."

Intel has dropped its request that the explanatory phrase "*e.g.*, converting or relocating a VMEbus address to a Futurebus address" be included in its proposed construction of this language. Thus, each side's proposed construction follows from its proposed construction of "mapping." In light of the court's construction of "mapping" above, no further construction is necessary.

### 5. "First Mapping Means"

<b>Term</b>	<b>VIA &amp; Intel's Proposal</b>	<b>CCCC's Proposal</b>
"first mapping means"	The corresponding structure cannot be precisely determined due to the indefiniteness of the claim element "means for asserting an indicating signal" and the inadequacies in the specification. To the extent any corresponding structure can be identified for the remaining functions of the element, it generally includes the interface circuit, including particularly the V-F translation circuit and Futurebus, as shown in Figures 1 and 2, and equivalents thereof.	In the specification of the '369 patent, structure(s) for performing the function(s) recited in this claim limitation is/are the circuitry described as the mapping circuit, V-F TRANSLATION 18 and Address Generator 47 and equivalents thereof.

The parties agree that "first mapping means" is a means-plus-function limitation. Defendants, however, contend that this clause is indefinite. "Under 35 U.S.C. § 112 ¶ 2 and ¶ 6, a means-plus-function clause is indefinite if a person of ordinary skill in the art would be unable to recognize the structure in the specification and associate it with the corresponding function in the claim." *Allvoice Computing PLC v. Nuance Communications, Inc.*, \_\_\_ F.3d \_\_\_, 2007 WL 2963933, \*3 (Fed. Cir. 2007).

Claim 1 recites, in relevant part, a:

first mapping means coupled to said first bus

for mapping first addresses within the first address space to second addresses within the second address space, for asserting an indicating signal and for generating one of said second addresses in response to one of said first addresses transmitted on said first bus from one of said first plurality of bus masters, said first mapping means also generating a SNOOP signal of a state indicating when a generated second address is mapped to one of said particular subset of the second data storage locations

'369 patent at 13:16-14:2. The "first mapping means" has four separate functions: (1) mapping first addresses to second addresses, (2) asserting an indicating signal, (3) generating second addresses in response to first addresses transmitted on the first bus from a first bus master, and (4) generating a SNOOP signal.

CCCC argues that the following portion of the summary of the invention section of the specification links the functions of the mapping means to the structure of the "mapping circuit":

[T]he interface circuit includes a mapping circuit that maps each of a set of VMEbus addresses to corresponding Futurebus addresses. When a computer processor on the VMEbus attempts to read or write access any one of the set of VMEbus addresses, the mapping circuit generates a corresponding Futurebus address and a SNOOP signal indicating whether the Futurebus address references a cached data storage location on the Futurebus.

'369 patent at 2:15-23. The first sentence of this passage links the "mapping circuit" to function (1), while the last sentence of this passage links the "mapping circuit" to functions (3) and (4). However, this particular passage does not discuss the "asserting" of function (2). As the Federal Circuit stated in *Medical Instrumentation & Diagnostics Corp. v. Elekta AB*:

The public should not be required to guess as to the structure for which the patentee enjoys the right to exclude. The public instead is entitled to know precisely what kind of structure the patentee has selected for the claimed functions, when claims are written according to section 112, paragraph 6. . . . If our interpretation of the statute results in a slight amount of additional written description compared with total omission of structure, that is the trade-off necessitated by an applicant's use of the statute's permissive generic means term.

344 F.3d 1205, 1220 (Fed. Cir. 2003) (quoting, in part, *Atmel Corp. v. Info. Storage Devices*, 198 F.3d 1374, 1382 (Fed. Cir. 1999)).

Of course, section 112 ¶ 6 cannot be satisfied when there is a total omission of structure. *Atmel*, 198 F.3d at 1378. However, the patent specification must be read as a whole to determine structure capable of performing the function claimed in a means plus-function limitation. *Budde v. Harley-Davidson, Inc.*, 250 F.3d 1369, 1379 (Fed. Cir. 2001). The corresponding structure need not

1 include all things necessary to enable the claimed invention to work, rather it must include all  
2 structure that actually performs the recited function.

3 Here, upon reading the patent specification as a whole it is apparent that the mapping circuit  
4 is the general structure within the disclosed interface circuit that corresponds to the first mapping  
5 means. Although the specification does not explicitly link the mapping circuit to a specific  
6 structure, it is unmistakable that V-F translation circuit 18 and address generator 47 together  
7 constitute a preferred embodiment describing the mapping circuit.<sup>6</sup>

8 The "mapping circuit" comprised of the V-F translation circuit 18 and address generator 47 is  
9 associated with the first bus (VMEbus) in the preferred embodiment. The preferred embodiment and  
10 the figures clearly describe and illustrate that the mapping circuit performs all four functions that a  
11 mapping means is claimed to perform in claim 1. The mapping circuit (1) maps the first addresses to  
12 second addresses by establishing a correspondence as defined above under "mapping," (2) asserts an  
13 indicating signal (specifically, V-LREQ as discussed below in "indicating signal"), (3) generates a  
14 second address in response to a first address transmitted on the first bus from a first bus master, and  
15 (4) generates a SNOOP signal. Figure 5, which illustrates these functions performed by the V-F  
16 translation circuit, is especially helpful in determining that this structure is the mapping means.

17 The court thus concludes that term "first mapping means" is not indefinite. As set forth  
18 above, the function of the "first mapping means" is as follows: "(1) mapping the first addresses to  
19 second addresses, (2) asserting an indicating signal, (3) generating a second address in response to a  
20 first address transmitted on the first bus from a first bus master, and (4) generating a SNOOP signal"  
21 and its structure is "the V-F translation circuit 18 and address generator 47 and equivalents thereof."  
22  
23  
24  
25

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26 <sup>6</sup> The mapping circuit is broken into these two components in the preferred embodiment because the  
27 VMEbus address is broken up into an upper and lower portion in order to accomplish the mapping:  
28 V-F translation circuit 18 translates the upper portion of the address; address generator 47 translates  
the lower portion of the address.

6. "Indicating Signal"

<i>Term</i>	<i>VIA &amp; Intel's Proposal</i>	<i>CCCC's Proposal</i>
"indicating signal"	This term is indefinite. To the extent the Court opts to provide a construction, Intel and VIA offer the following alternative to CCCC's proposal: "a signal that triggers the actions of placing the generated second address together with the SNOOP signal on the second bus, receiving data from a second data storage location mapped to the generated second address, and transmitting the received data to a requesting bus master via a first bus."	"A signal that results when an address in a first address space has been mapped to an address in a second address space."

Via has separately moved for summary judgment that the patent is invalid for indefiniteness. It asserts, *inter alia*, that the term "indicating signal" cannot be construed because, aside from the claims, there is no other description of the "indicating signal" in the patent. This section addresses both Via's motion for summary judgment and the construction, if one is possible, of "indicating signal."

The term "indicating signal" appears as part of the first mapping means in the asserted claim as follows:

first mapping means coupled to said first bus for mapping first addresses within the first address space to second addresses within the second address space, for asserting an indicating signal and for generating one of said second addresses in response to one of said first addresses transmitted on said first bus from one of said first plurality of bus masters, said first mapping means also generating a SNOOP signal of a state indicating when a generated second address is mapped to one of said particular subset of the second data storage locations

'369 patent at 13:15-14:6 (emphasis added). The parties have agreed that "indicating signal" is part of a means-plus-function claim, thus the corresponding structure must be identified to construe this term. A challenge to a claim containing a means-plus-function limitation as lacking structural support requires a finding, by a clear and convincing evidence, that the specification lacks disclosure of structure sufficient to be understood by one skilled in the art as being adequate to perform the recited function. *Intell. Prop. Dev., Inc. v. UA-Columbia Cablevision of Westchester, Inc.*, 336 F.3d 1308, 1319 (Fed. Cir. 2003); *see also Allvoice Computing*, \_\_\_ F.3d at \_\_\_, 2007 WL 2963933, \*3. Where a means-plus-function claim is not "amenable to construction," it is invalid as indefinite

1 under 35 U.S.C. § 112 ¶ 2. *Exxon Research & Eng'g Co. v. United States*, 265 F.3d 1371, 1375  
2 (Fed. Cir. 2001).

3 The indicating signal must satisfy requirements set forth in the claims. First, it has to be  
4 asserted by the mapping means. Second, the bus interface means has to respond to this signal as  
5 described in the last paragraph of claim 1. '369 patent at 14:3-8 ("bus interface means connected to  
6 said first and second buses for responding to the first indicating signal when said on of said first  
7 plurality of bus masters is reading data . . .").

8 The first step to identifying which signal is the claimed "indicating signal" is determining  
9 which structure corresponds to the "mapping means" because pursuant to the claim language, the  
10 indicating signal is asserted by the mapping means. '369 patent at 13:16-19 ("first mapping means  
11 coupled to said first bus . . . for asserting an indicating signal . . ."). As discussed above, the  
12 structure that corresponds to the mapping means for asserting the indicating signal is the mapping  
13 circuit or, in the preferred embodiment, the V-F translation circuit or address generator.

14 In its motion for summary judgment, Via challenges the asserted claim as indefinite because,  
15 it argues, it is not clear what the "indicating signal" refers to. As set forth in the claims, however,  
16 the indicating signal indicates a request which then initiates a sequence of steps related to arbitration  
17 and control that results in placing the translated address onto the second bus. *See* '369 patent at  
18 14:3-12.

19 Via further contends that based on CCCC's proposed construction ("A signal that results  
20 when an address in a first address space has been mapped to an address in a second address space"),  
21 any number of the following signals discussed in the patent could be the indicating signal: the  
22 SNOOP signal, the V-LREQ request signal, the EN4 enable signal, the LOC\_AS local address  
23 strobe signal, the L-FREQ request signal, the EN6 enable signal, the BT block transfer indicating  
24 signal. However, of the candidate signals suggested by Via, only SNOOP, BT, and V-LREQ are  
25 asserted by the V-F translation circuit.

26 Of the signals asserted by the V-F translation circuit, SNOOP could not be the indicating  
27 signal because the claim specifically distinguishes between SNOOP and indicating signal. The  
28 claim states that one of the responses to an indicating signal is "placing the generated second address

1 and SNOOP signal on the second bus." '369 patent at 14:5-7. Because the SNOOP signal is placed  
2 in response to the indicating signal, these signals cannot be the same. The BT signal also cannot be  
3 the indicating signal because the BT signal only applies when VMEbus wishes to perform a block  
4 transfer wherein it read or write accesses a variable number of up to 256 data bytes at successive  
5 addresses on Futurebus, thus limiting it to a specific application. *See* '369 patent at 6:18-25.

6 It is suggested by both experts that V-LREQ may be the indicating signal. Indeed, this signal  
7 satisfies all the requirements that an indicating signal must have. It is asserted by the mapping  
8 circuit, it is understood to indicate a request to the VMEbus arbitration and control circuit, which  
9 then initiates a sequence of steps related to arbitration and control. The bus interface subsequently  
10 responds to this signal. This V-LREQ signal is shown in the patent figures as starting a cascade of  
11 commands that occur to place the translated address on the second bus. *See* Fig. 2. Thus, the court  
12 construes "indicating signal" as the "V-LREQ request signal" which is a signal that requests control  
13 of the first bus. *See* '369 patent at 5:5-28 ("V-F translation circuit **18** determines whether the VME  
14 address bus has been addressed to a corresponding Futurebus address, and if so, transmits a request  
15 signal V-LREQ to VMEbus arbitration and control circuit **38**").

<i>Term</i>	<i>VIA &amp; Intel's Proposal</i>	<i>CCCC's Proposal</i>
"responding to the first indicating signal when said one of said first plurality of bus masters is reading data by placing the generated second address and SNOOP signal on the second bus"	"responding to the first indicating signal when one of the bus masters connected to the first bus has initiated a read transaction by placing the generated second address together with the SNOOP signal on the second bus."	"Responding to the indicating signal when a bus master is reading data by placing an address and a SNOOP signal on the second bus."

23 Via separately asserts in its motion for summary judgment that because there is no "second  
24 indicating signal," the "first indicating signal" referenced in this disputed language, claim 1 is  
25 indefinite. The court does not find this argument persuasive. As set forth above, the patent  
26 specification does not refer to an indicating signal. "Indicating signal" appears twice in claim 1:  
27 "first mapping means . . . for asserting an indicating signal . . ." and "bus interface means . . . for  
28 responding to the first indicating signal." '269 patent at 13:16-19; 14:3-4. CCCC has presented

evidence that a person of ordinary skill in the art would readily understand that the "first indicating signal" is in reference to the prior use of "indicating signal" in claim 1. Dubois Decl. (dkt. # 160) ¶ 13. Via presents no evidence to the contrary.

Further, neither side's proposal provides any particularly helpful clarification to the claim language at issue. However, as CCCC's proposed construction eliminates any reference to the "first plurality of bus masters," the court feels it necessary to construe the use of "first" and "second" in this disputed claim language. Consistent with its discussion of "first" and "second" above in conjunction with the construction of "address space," the court construes "responding to the first indicating signal when said one of said first plurality of bus masters is reading data by placing the generated second address and SNOOP signal on the second bus" to mean "responding to the indicating signal from the first bus when one of the bus masters connected to the first bus is reading data by placing the generated second address and SNOOP signal on the second bus."<sup>7</sup>

#### 7. Bus Interface Means

<i>Term</i>	<i>VIA &amp; Intel's Proposal</i>	<i>CCCC's Proposal</i>
"bus interface means"	To the extent any corresponding structure can be identified, it generally includes circuitry within the interface circuit 8.	In the specification of the '369 patent, structure(s) for performing the function(s) recited in this claim limitation are the circuitry described as buffer 22, local bus 16, buffer 49, buffer 24, buffer 36, local bus 14, buffer 32 and Futurebus Arbitration and Control 40 in interface circuit 8 shown in Figure 2 and equivalents thereof.

As with the "first mapping means," the parties agree that "bus interface means" is a means-plus-function limitation with multiple functions. Defendants contend, however, that there is no corresponding structure disclosed in the specification and that, accordingly, the claim is invalid as indefinite. Claim 1 recites a:

bus interface means connected to said first and second buses for responding to the first indicating signal when said one of said first plurality of bus masters is reading data by placing the generated second address and SNOOP signal on the second bus,

<sup>7</sup> The court notes that elsewhere in claim 1 is recited "said second bus including means for conveying a SNOOP signal *with* an address appearing on the bus." '369 patent at 13:9-11 (emphasis added).

1 receiving data from a second data storage location mapped to said second address,  
2 and transmitting the received data to said one of said first plurality of bus masters via  
said first bus when the said one of said first plurality of bus masters is reading data.

3 '369 patent at 14:3-12. The "bus interface means" thus has three separate functions: (1) responding  
4 to the first indicating signal when a first bus master reads data by placing the generated second  
5 address and SNOOP signal on the second bus, (2) receiving data from a memory on the second bus,  
6 and (3) transmitting the received data to a first bus master.

7 The corresponding structure in the specification is identified as a general structure, the "bus  
8 interface circuit." '369 patent at 2:22. CCCC identifies a collection of structures that comprise the  
9 "bus interface means." The portions of the interface circuit **8** that CCCC argues make up the "bus  
10 connection means" are set forth in Figure 2.

11 As CCCC asserts, buffer **22**, buffer **24**, buffer **32**, buffer **36**, buffer **49**, local data buses **14**  
12 and **16**, and Futurebus arbitration and control circuit **40** collectively make up the structure associated  
13 with function (1). Responding to the first indicating signal, which the court has construed to be the  
14 V-LREQ request signal, involves returning the data requested by the first bus master when it places  
15 the mapped addresses on the second bus through buffer **22**, buffer **49**, buffer **24**, buffer **36**, local data  
16 bus **14**, buffer **32**, and Futurebus arbitration and control circuit **40**. *See* '369 patent at 4:11-37 & fig.  
17 2.

18 CCCC identifies a subset of the parts associated with function (1)—buffer **32**, buffer **36**,  
19 local data bus **14**, and Futurebus arbitration and control circuit **40**—that collectively make up the  
20 structure associated with functions (2) and (3). Indeed, "receiving" and "transmitting" both involve  
21 sending the requested data to the first bus through buffer **36**, local data bus **14**, buffer **32**, and  
22 Futurebus arbitration and control circuit **40**.

23 The court thus concludes that term "bus interface means" is not indefinite. As set forth  
24 above, the function of the "bus interface means" is as follows: "(1) responding to the first indicating  
25 signal when a first bus master reads data by placing the generated second address and SNOOP signal  
26 on the second bus, (2) receiving data from a memory on the second bus, and (3) transmitting the  
27 received data to a first bus master" and its structure is "buffer **22**, buffer **49**, buffer **24**, buffer **36**,  
28

local data buses **14** and **16**, buffer **32**, and Futurebus arbitration and control circuit **40** and equivalents thereof."

### III. ORDER

For the foregoing reasons, the court

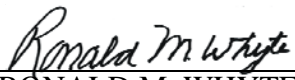
1. adopts the following construction of terms in the '369 patent:

<i><b>Term</b></i>	<i><b>Construction</b></i>
"bus"	"A signal line or set of signal lines used by an interface system to connect a number of devices and to transfer information between the devices."
"address space", "first address space", "second address space"	"A set of addresses." "First address space" is an address space that necessarily refers to addresses represented on the first bus; "second address space" is an address space that necessarily refers to addresses represented on the second bus.
"SNOOP signal"	"A signal indicating whether an address references a cached data storage location."
"the SNOOP signal telling said one of said second plurality of bus masters when to write cached data to the address appearing on the bus"	"The SNOOP signal indicating to one of the bus masters on the second bus when to write cached data to the one of the second data storage locations at the address appearing on the second bus."
"a SNOOP signal of a state indicating when a generated second address is mapped to one of said particular subset of the second data storage locations"	(no construction necessary)
"said second bus including means for conveying a SNOOP signal with an address appearing on the bus"	"A second bus with the function of conveying a SNOOP signal with an address appearing on the bus and having the structure of a Futurebus or its equivalents."
"mapping"	"Establishing a correspondence between the elements of one set and elements of another set."
"mapping first addresses within the first address space to second addresses within the second address space"	(no construction necessary)
"first mapping means"	Function: (1) mapping the first addresses to second addresses, (2) asserting an indicating signal, (3) generating a second address in response to a first address transmitted on the first bus from a first bus master, and (4) generating a SNOOP signal. Structure: the V-F translation circuit 18 and address generator 47 and equivalents thereof.
"indicating signal"	"V-LREQ request signal" which is a signal that requests control of the first bus.
"responding to the first indicating signal when said one of said first plurality of bus masters is reading data by placing the generated second address and SNOOP signal on the second bus"	"Responding to the indicating signal when one of the bus masters connected to the first bus is reading data by placing the generated second address and SNOOP signal on the second bus."

<b>Term</b>	<b>Construction</b>
"bus interface means"	Function: (1) responding to the first indicating signal when a first bus master reads data by placing the generated second address and SNOOP signal on the second bus, (2) receiving data from a memory on the second bus, and (3) transmitting the received data to a first bus master. Structure: buffer 22, buffer 49, buffer 24, buffer 36, local data buses 14 and 16, buffer 32, and Futurebus arbitration and control circuit 40 and equivalents thereof.

2. sustains defendants' objections to the January 15, 2007 declaration of Omer Salik (dkt. # 198);  
and
3. denies Via's motion for summary judgment that the '369 patent is invalid as indefinite.

DATED: 10/22/07

  
RONALD M. WHYTE  
United States District Judge

